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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,530	11/30/2001	Paul L. Master	QuickSilver Technology, I	6090

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,530	MASTER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2002*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-99* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 1-99 are subject to the restriction requirements.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-31 , drawn to a system for adapting configuration including g interconnection network, and a plurality of heterogeneous computational elements having fixed architecture, classified in class 709, subclass 221.

II. Claims 32-62, drawn to a method of receiving the first set of configuration information including a first subset of information and second subset of information , classified in class 370, subclass 415.

III. Claims 63-88, drawn to a method for transmitting the first set of configuration information including a first subset of information and second subset of information , classified in class 370, subclass 473.

IV. Claims 89-90 , drawn to an adaptive integrated circuit including matrix interconnection network coupled to a plurality of reconfigurable matrices, classified in class 340, subclass 2.2.

V. Claims 91-92, drawn to an integrated circuit including heterogeneous computational elements configured for a controller operating mode and the second subset of heterogeneous computational elements configured

for a memory operating mode and the scheduling of the configuration and reconfiguration, classified in class 712, subclass 43.

VI. Claims 93 , drawn to an integrated circuit including first and second fixed architectures which are different including functions for memory, addition, multiplication, complex multiplication, subtraction, and field programmability, classified in class 708, subclass 490.

VII. Claims 94-99 , drawn to an adaptive integrated circuit comprising a plurality of fixed and differencing computational elements , classified in class 714, subclass 43.

2. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a system which does not have a method of receiving the first set of configuration information including a first subset of information and second subset of information. See MPEP § 806.05(d).

3. Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such

as a system which does not have a method of transmitting the first set of configuration information including a first subset of information and second subset of information. See MPEP § 806.05(d).

4. Inventions I and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a system which does not have an adaptive integrated circuit including matrix interconnection network coupled to a plurality of reconfigurable matrices. See MPEP § 806.05(d).

5. Inventions I and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a system which does not have an integrated circuit including heterogeneous computational elements configured for a controller operating mode and the second subset of heterogeneous computational elements configured for a memory operating mode. See MPEP § 806.05(d).

6. Inventions I and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a system which does not have an integrated circuit including first and second fixed architectures which are different including the functions for memory, addition,

multiplication, complex multiplication, subtraction, and field programmability. See MPEP § 806.05(d).

7. Inventions I and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a system which does not have an adaptive integrated circuit including a plurality of fixed and differencing computational elements . See MPEP § 806.05(d).

8. Inventions II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as a method which does not have the transmit ion of the first set of configuration information including a first subset of information and second subset of information. See MPEP § 806.05(d).

9. Inventions II and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as a method which does not have an adaptive integrated circuit including matrix interconnection network coupled to a plurality of reconfigurable matrices. See MPEP § 806.05(d).

10. Inventions II and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such

as a method which does not have an adaptive integrated circuit including heterogeneous computational elements configured for a controller operating mode and the second subset of heterogeneous computational elements configured for a memory operating mode. See MPEP § 806.05(d).

11. Inventions II and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as a method which does not have adaptive integrated circuit including first and second fixed architectures which are different including functions for memory, addition, multiplication, complex multiplication, subtraction, and field programmability. See MPEP § 806.05(d).

12. Inventions II and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as a method which does not have an adaptive integrated circuit including a plurality of fixed and different computational elements . See MPEP § 806.05(d).

13. Inventions III and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as a method which does not have an adaptive integrated circuit including

matrix interconnection network coupled to a plurality of reconfigurable matrices. See MPEP § 806.05(d).

14. Inventions III and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as a method which does not have an adaptive integrated circuit include g heterogeneous computational elements configured for a controller operating mode and the second subset of heterogeneous computational elements configured for a memory operating mode . See MPEP § 806.05(d).

15. Inventions III and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as a method which does not have an adaptive integrated circuit including first and second fixed architectures which are different including functions for memory, addition, multiplication, complex multiplication, subtraction, and field programmability. See MPEP § 806.05(d).

16. Inventions III and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention III has separate utility such as a method which does not have an adaptive integrated circuit comprising a plurality of fixed and different computational elements . See MPEP § 806.05(d).

17. Inventions IV and V are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention IV has separate utility such as a system which does not including heterogeneous computational elements configured for a controller operating mode and the second subset of heterogeneous computational elements configured for a memory operating mode. See MPEP § 806.05(d).

18. Inventions IV and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention IV has separate utility such as a system which does not including first and second fixed architectures which are different including functions for memory, addition, multiplication, complex multiplication, subtraction, and field programmability. See MPEP § 806.05(d).

19. Inventions IV and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VII has separate utility such as a system which does not have matrix interconnection network coupled to a plurality of reconfigurable matrices. See MPEP § 806.05(d).

20. Inventions V and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention V has separate utility such

as a system which does not have first and second fixed architectures which are different including functions for memory, addition, multiplication, complex multiplication, subtraction, and field programmability,. See MPEP § 806.05(d).

21. Inventions V and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VII has separate utility such as a system which does not have first computational elements configured for a controller operating mode and the second subset of heterogeneous computational elements configured for a memory operating mode and the scheduling of the configuration and reconfiguration. See MPEP § 806.05(d).

22. Inventions VI and VII are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention VI has separate utility such as a system which does not have a plurality of fixed and different computational elements. Invention VI is directed to computational elements having fixed architectures which are different (see claim 93, lines 10-15) while invention VII is directed to fixed and different computational elements (see claim 94, lines 3-7) The fixed architectures which are different does not mean the computational elements are fixed and different. See MPEP § 806.05(d).

23. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

24. Because these inventions are distinct for the reasons given above and the search required, for example, Group VI is not required for Group VII , restriction for examination purposes as indicated is proper. Invention VI is directed to computational elements having fixed architectures which are different (see claim 93, lines 10-15) while invention VII is directed to fixed and different computational elements (see claim 94, lines 3-7). The fixed architectures which are different does not mean the computational elements are fixed and different. Therefore, search required for The fixed architectures which are different is not required for fixed and different computational elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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